WHAT IS CLAIMED IS:

1. A method for processing integrated circuit devices, the method comprising:

providing a monitor wafer, the monitor wafer comprising a silicon material;

introducing a plurality of particles within a depth of the silicon material, whereupon the plurality of particles have a reduced activation energy within the silicon material;

subjecting the monitor wafer including the plurality of particles into a rapid thermal anneal process;

applying the rapid thermal anneal process at a first state including a first temperature, the first temperature being within a range defined as a low temperature range, the low temperature range being less than 650 Degrees Celsius;

removing the monitor wafer;

measuring a sheet resistivity of the monitor wafer;

determining the first temperature within a tolerance of less than 2 percent across the monitor wafer; and

operating the rapid thermal process using a plurality of production wafers if the first temperature is within a tolerance of a specification temperature.

2. The method of claim 1 wherein the introducing of particles comprising:

implanting silicon bearing impurities into the silicon material to cause the silicon material to be in an amorphous state; and

implanting boron bearing impurities into the silicon material, whereupon the boron bearing impurities are free from activation as applied to the silicon material.

3. The method of claim 2 wherein the silicon bearing impurities are implanted using a dose of 1×10^{14} atoms/cm^2.

4. The method of claim 2 wherein the boron bearing impurities are implanted using a dose of 3.5×10^{15} atoms/cm^2.

5. The method of claim 1 wherein the first temperature is less than 650 Degrees Celsius.

6. The method of claim 1 wherein the first temperature is less than 550 Degrees Celsius.

7. The method of claim 1 wherein the silicon material is in an amorphous state upon deposition.

8. The method of claim 1 wherein the sheet resistivity is provided in a separate tool.

9. The method of claim 1 wherein the operating of the production wafers occurs for 24 hours.

10. The method of claim 1 wherein the monitor wafer is characterized by a temperature sensitivity of at least 1 Ohms per Degree Celsius.

11. A method for processing integrated circuit devices, the method comprising:

providing a monitor wafer, the monitor wafer comprising a silicon material having a thickness to a predetermined depth;

implanting silicon bearing impurities into the silicon material to cause the silicon material to be in an amorphous state within a portion of the thickness of the silicon material;

implanting boron bearing impurities into the silicon material within at least the portion of thickness in the amorphous state, whereupon the boron bearing impurities are free from activation as applied to the silicon material and have a reduced activation energy within the silicon material;

subjecting the monitor wafer including the silicon bearing impurities and boron bearing impurities into a rapid thermal anneal process;

applying the rapid thermal anneal process at a first state including a first temperature to activate a portion of the boron bearing impurities, the first temperature being within a range defined as a low temperature range, the low temperature range being less than 650 Degrees Celsius;

removing the monitor wafer;

measuring a sheet resistivity of the monitor wafer;

determining the first temperature within a tolerance of less than 2 percent across the monitor wafer; and

operating the rapid thermal process using a plurality of production wafers if the first temperature is within a tolerance of a specification temperature.

12. The method of claim 11 wherein the activated boron bearing impurities influence the sheet resistivity.

13. The method of claim 11 wherein the monitor wafer comprising the boron bearing impurities and the silicon bearing impurities are characterized by a temperature sensitivity of at least 1 Ohms per Degree Celsius.

14. The method of claim 11 wherein the range being less than 550 Degrees Celsius.

15. The method of claim 11 wherein the silicon bearing impurities are implanted using a dose of 1×10^{14} atoms/cm^2.

16. The method of claim 11 wherein the boron bearing impurities are implanted using a dose of 3.5×10^{15} atoms/cm^2.

17. The method of claim 11 wherein the tolerance of the temperature specification is less than 1 percent across the monitor wafer.

18. The method of claim 11 wherein the plurality of production wafers is at least 100 wafers.

19. The method of claim 11 wherein the monitor wafer is a silicon wafer.

20. The method of claim 11 further comprising storing the monitor wafer after the boron implanting and silicon implanting.